FIG. 1

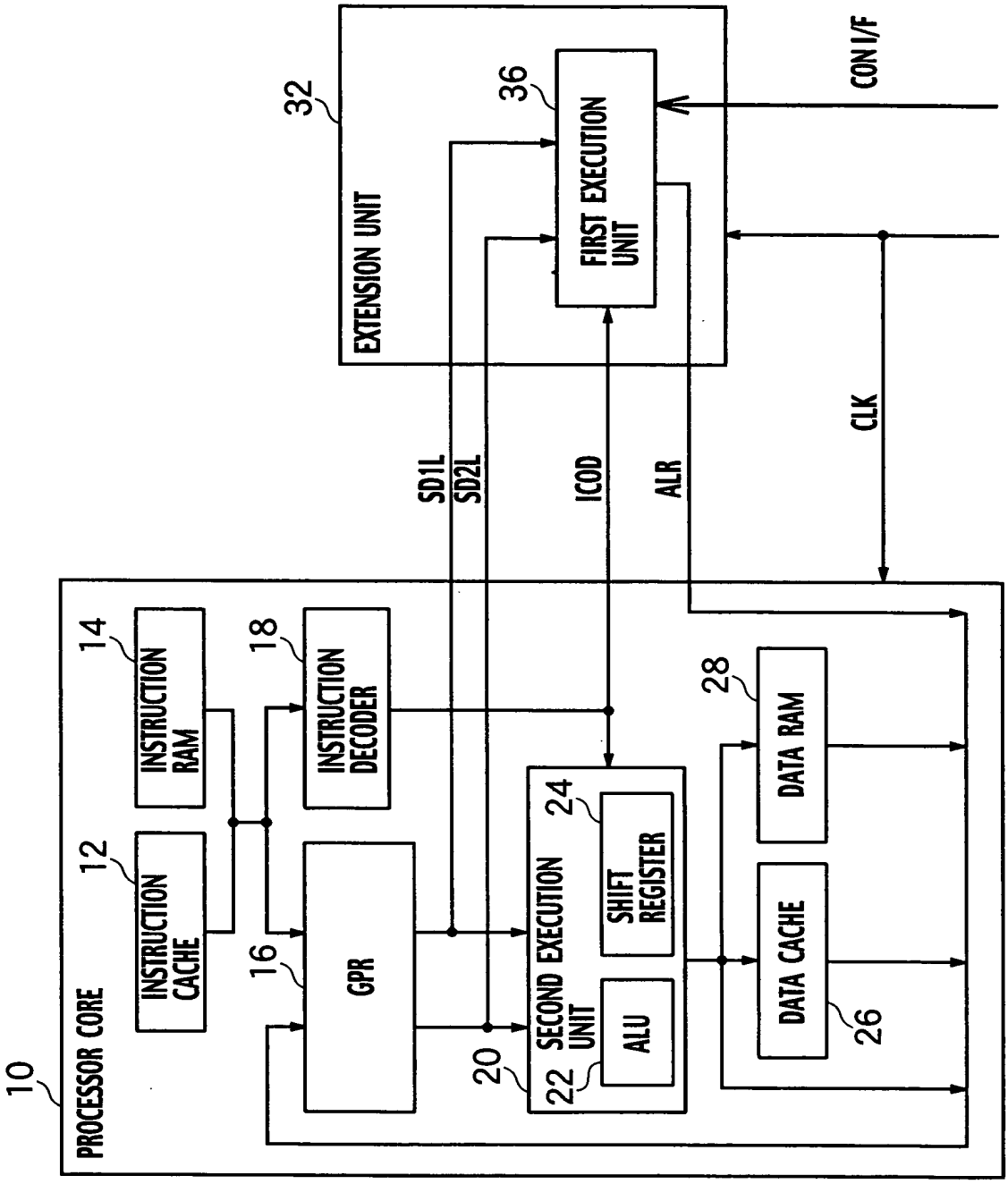

10
PROCESSOR CORE
12
INSTRUCTION CACHE
14
INSTRUCTION RAM
16
GPR
18
INSTRUCTION DECODER
20
22
SECOND EXECUTION UNIT
ALU
24
SHIFT REGISTER
26
DATA CACHE
28
DATA RAM
32
EXTENSION UNIT
36
FIRST EXECUTION UNIT
CON I/F
CLK
ALR
ICOD
SD2L
SD1L

FIG. 2

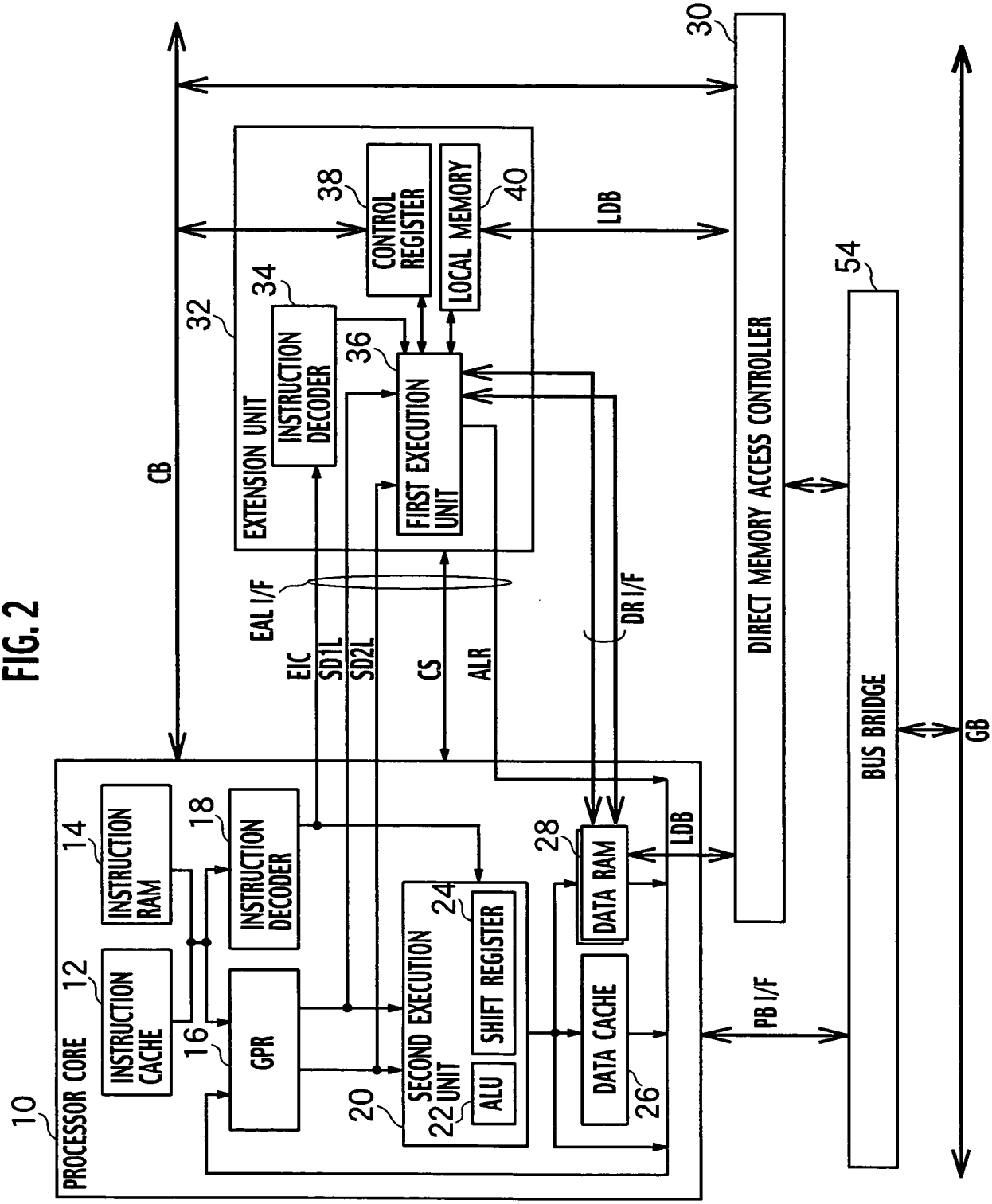

10
PROCESSOR CORE
12
INSTRUCTION CACHE
14
INSTRUCTION RAM
16
GPR
18
INSTRUCTION DECODER
20
SECOND EXECUTION UNIT
22
ALU
24
SHIFT REGISTER
26
DATA CACHE
28
DATA RAM
30
DIRECT MEMORY ACCESS CONTROLLER
32
EXTENSION UNIT
34
INSTRUCTION DECODER
36
FIRST EXECUTION UNIT
38
CONTROL REGISTER
40
LOCAL MEMORY
54
BUS BRIDGE
CB
LDB
EAL I/F
EIC
SD1L
SD2L
CS
ALR
DR I/F
PB I/F
GB

FIG. 3

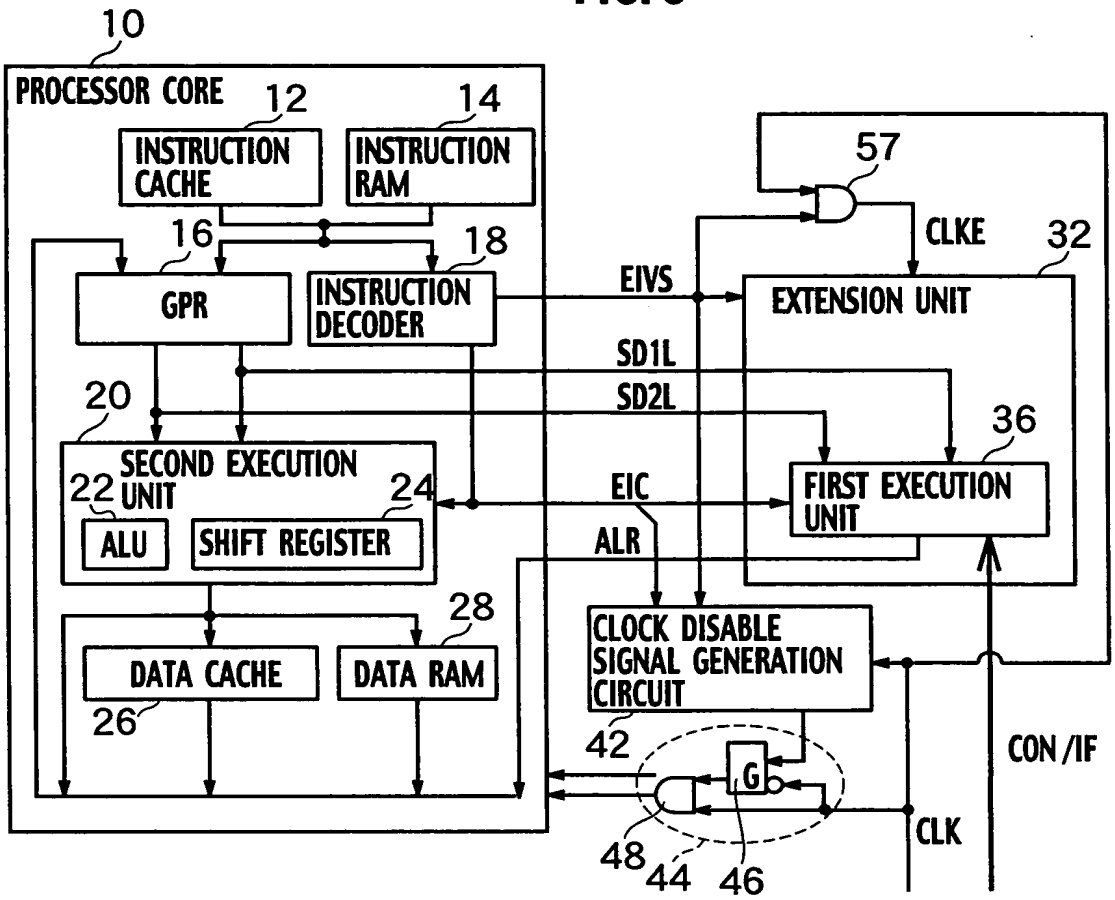

10
PROCESSOR CORE
12
INSTRUCTION CACHE
14
INSTRUCTION RAM
16
GPR
18
INSTRUCTION DECODER
20
SECOND EXECUTION UNIT
22
ALU
24
SHIFT REGISTER
26
DATA CACHE
28
DATA RAM
57
CLKE
32
EXTENSION UNIT
EIVS
SD1L
SD2L
36
FIRST EXECUTION UNIT
EIC
ALR
CLOCK DISABLE SIGNAL GENERATION CIRCUIT
42
G
CON/IF
CLK
48
44
46

FIG. 4

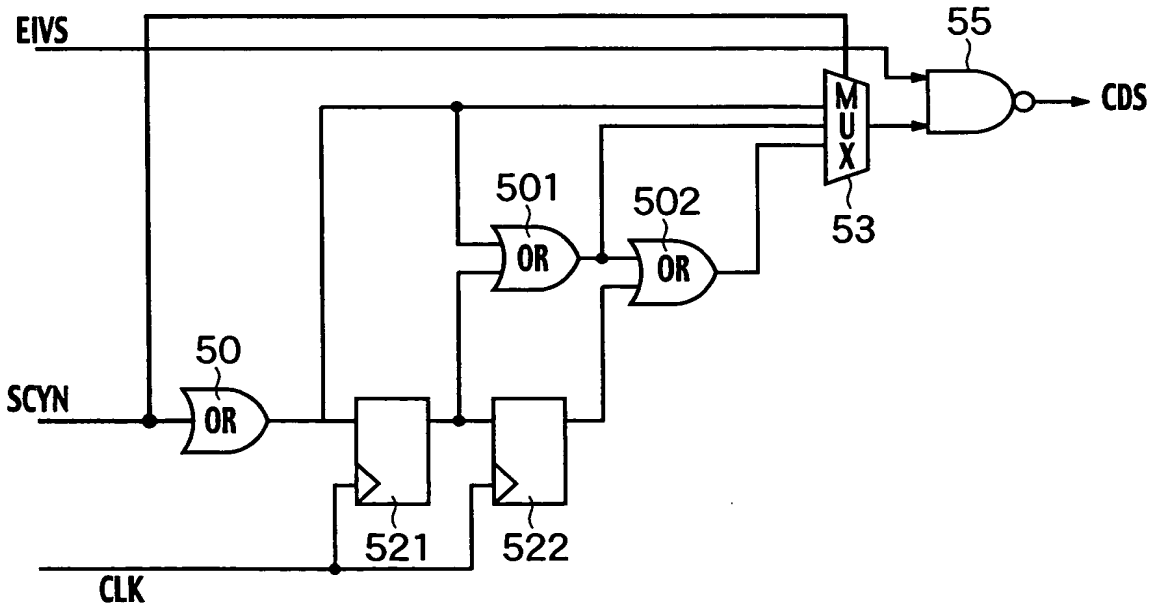

EIVS
55
CDS
MUX
53
501
OR
502
OR
50
SCYN
OR
521
522
CLK

FIG. 5

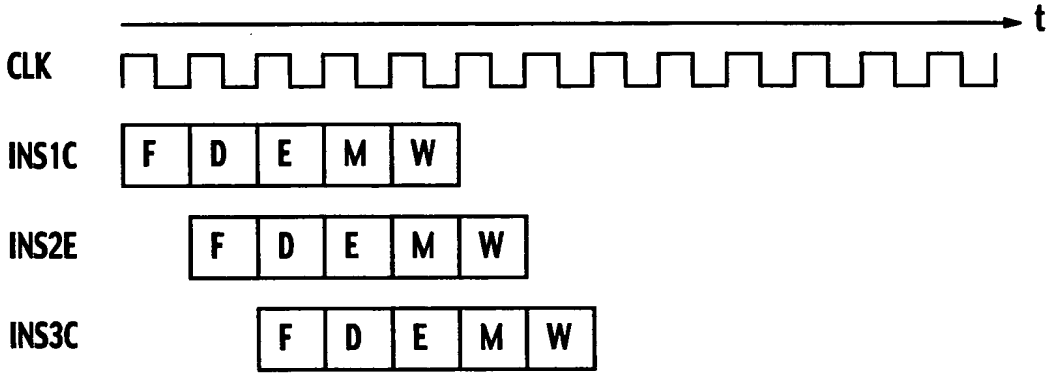

t
CLK
INS1C
F D E M W
INS2E
F D E M W
INS3C
F D E M W

FIG. 6

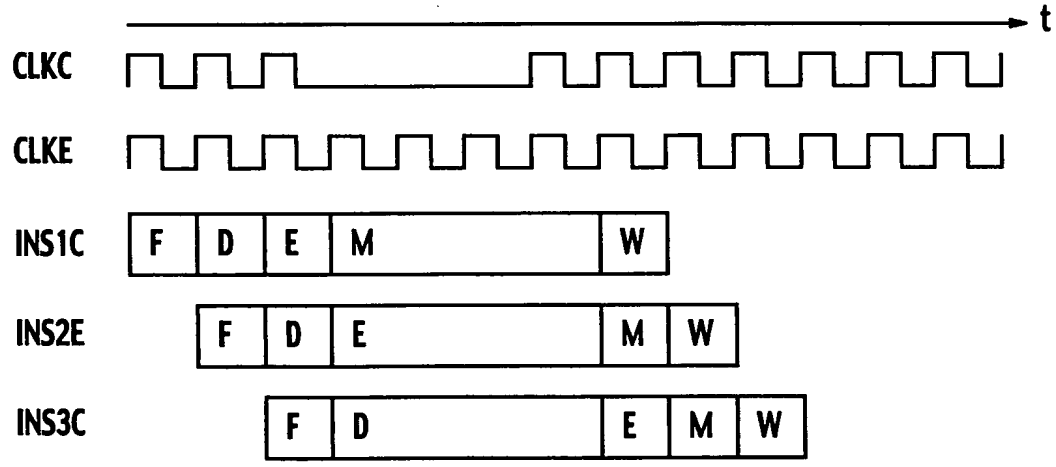

t
CLKC
CLKE
INS1C
F D E M W
INS2E
F D E M W
INS3C
F D E M W

FIG. 7

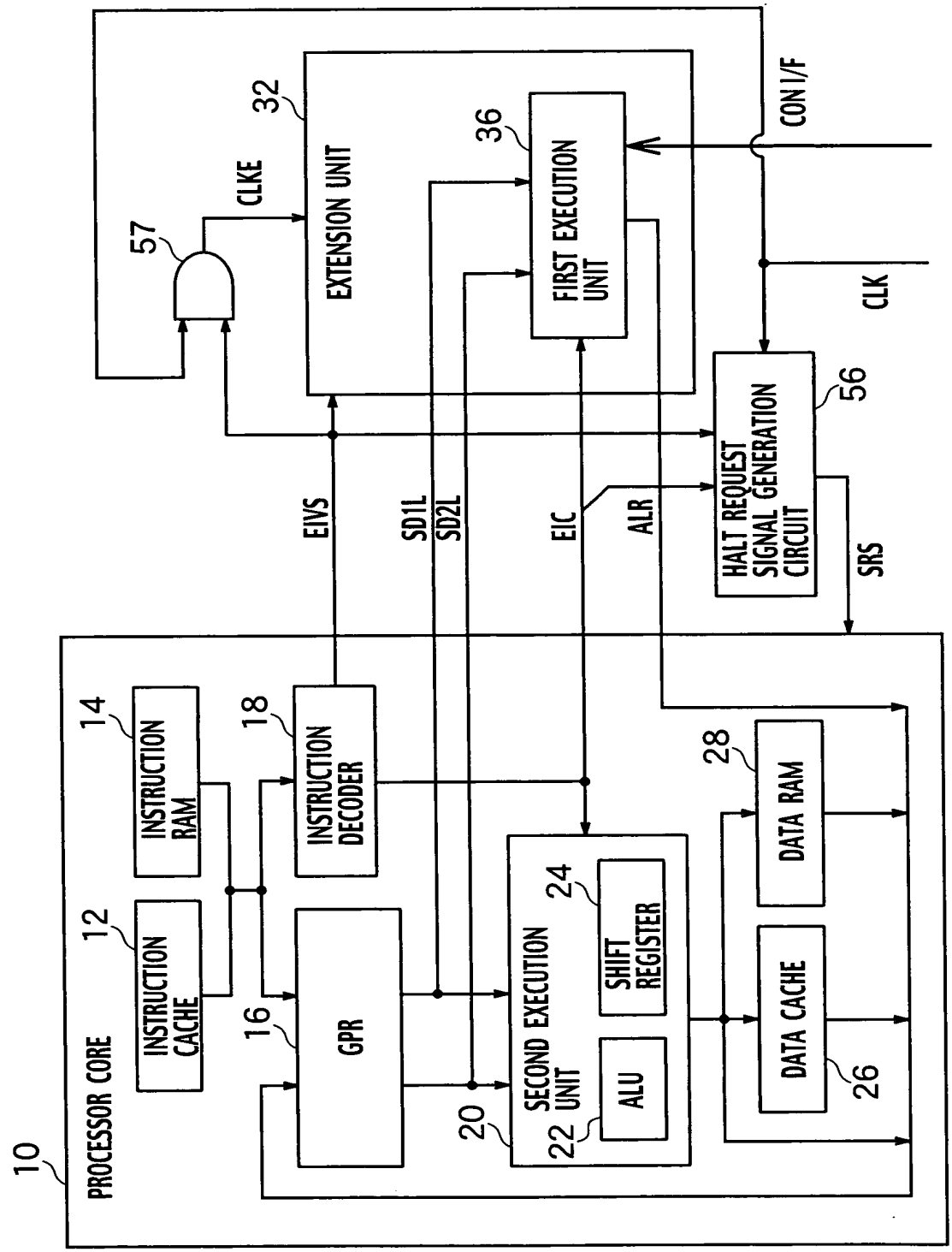

10
PROCESSOR CORE
12
INSTRUCTION CACHE
14
INSTRUCTION RAM
16
GPR
18
INSTRUCTION DECODER
20
SECOND EXECUTION UNIT
22
ALU
24
SHIFT REGISTER
26
DATA CACHE
28
DATA RAM
32
EXTENSION UNIT
36
FIRST EXECUTION UNIT
56
HALT REQUEST SIGNAL GENERATION CIRCUIT
57
CLKE
CON I/F
CLK
EIVS
SD1L
SD2L
EIC
ALR
SRS

FIG. 8

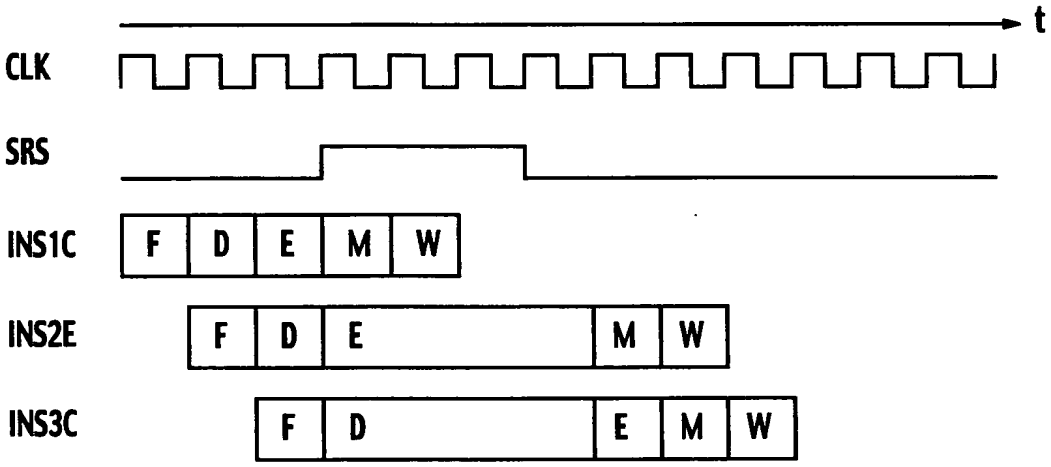

t
CLK
SRS
INS1C
F
D
E
M
W
INS2E
F
D
E
M
W
INS3C
F
D
E
M
W

FIG. 9

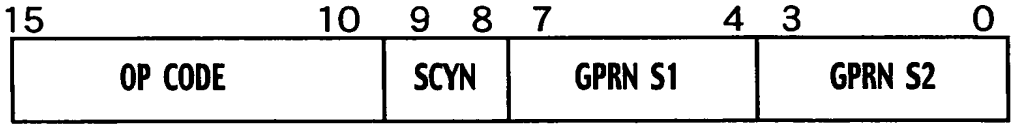

15
10
9
8
7
4
3
0
OP CODE
SCYN
GPRN S1
GPRN S2

FIG. 10

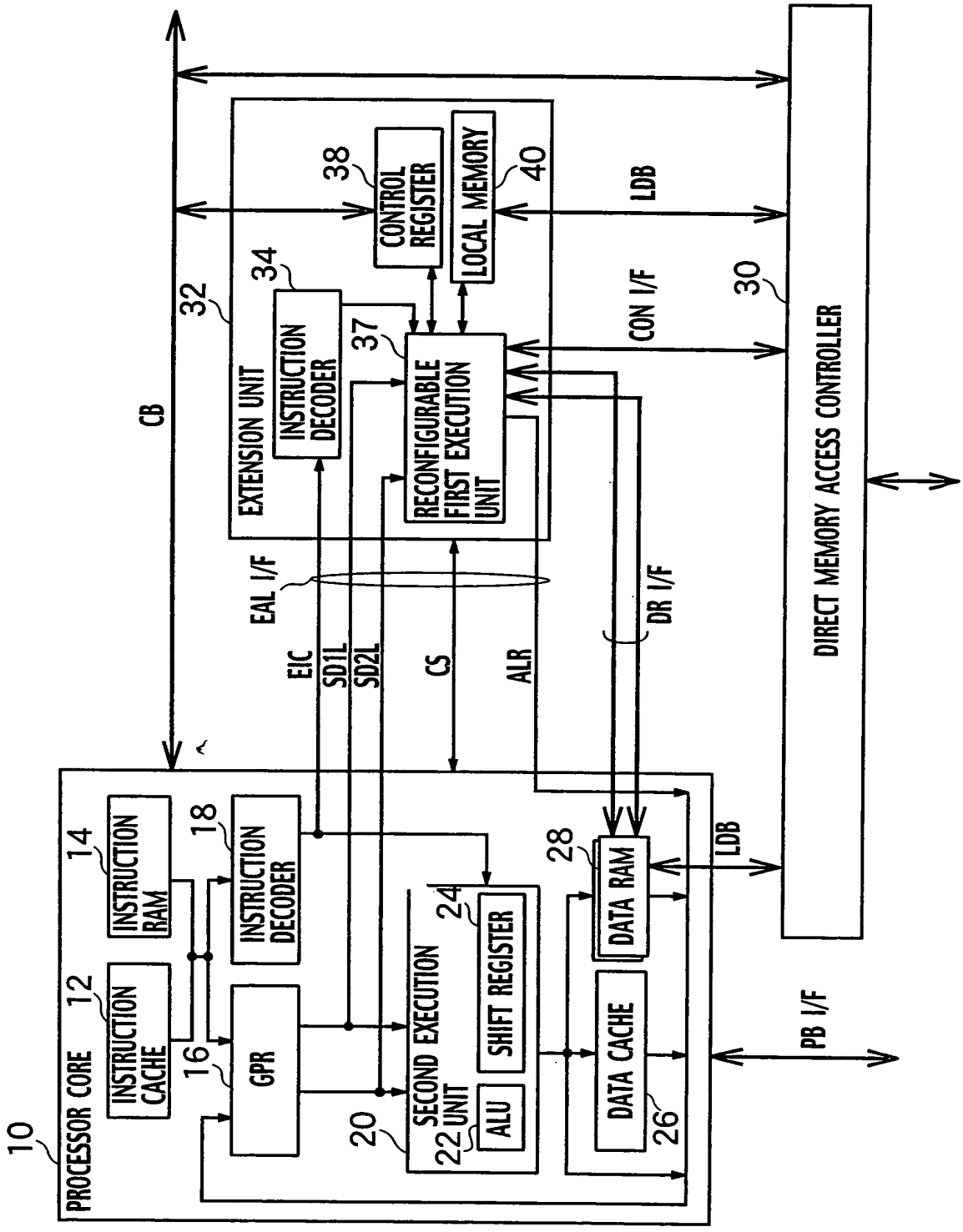
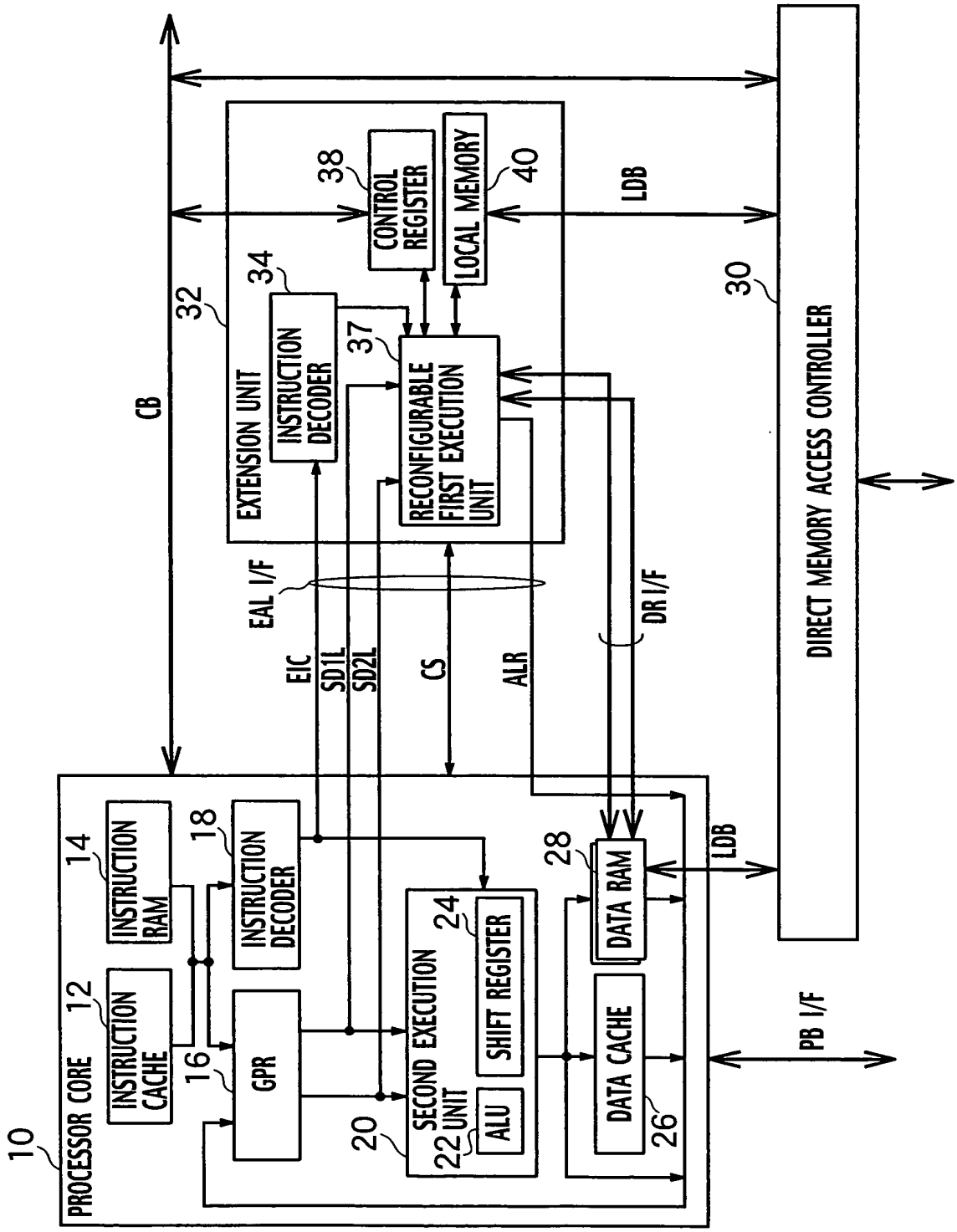

PROCESSOR CORE
10
INSTRUCTION CACHE
12
INSTRUCTION RAM
14
GPR
16
INSTRUCTION DECODER
18
SECOND EXECUTION UNIT
20
ALU
22
SHIFT REGISTER
24
DATA CACHE
26
DATA RAM
28
DIRECT MEMORY ACCESS CONTROLLER
30
CB
32
EXTENSION UNIT
INSTRUCTION DECODER
34
RECONFIGURABLE FIRST EXECUTION UNIT
37
CONTROL REGISTER
38
LOCAL MEMORY
40
LDB
CON I/F
EAL I/F
DR I/F
PB I/F
EIC
SD1L
SD2L
CS
ALR

FIG. 11


PROCESSOR CORE
10
INSTRUCTION CACHE
12
INSTRUCTION RAM
14
GPR
16
INSTRUCTION DECODER
18
SECOND EXECUTION UNIT
20
ALU
22
SHIFT REGISTER
24
DATA CACHE
26
DATA RAM
28
DIRECT MEMORY ACCESS CONTROLLER
30
CB
EXTENSION UNIT
32
INSTRUCTION DECODER
34
RECONFIGURABLE FIRST EXECUTION UNIT
37
CONTROL REGISTER
38
LOCAL MEMORY
40
LDB
EAL I/F
EIC
SD1L
SD2L
CS
ALR
DR I/F
PB I/F